REMARKS

Claim 23 stands rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors, at the time the application was filed, had possession of the claimed invention. Particularly, the Examiner states that the limitation of "a thickness sufficient to permit nucleation that forms nanometer size particles and small enough to prevent formation of a continuous layer" has no positive support in the specification. Applicants respectfully traverse the rejection.

Initially, Applicant's respectfully submit that the claim language is sufficient because an artisan would understand the claims. Further, the claim language itself defines specific conditions, mainly "a thickness sufficient to permit nucleation that forms nanometer size particles" and "small enough to prevent formation of a continuous layer," that reasonably convey to the artisan that the inventors had possession of the claimed invention. An artisan would understand this limitation even without the written description. Nanometer size particles may be observed, as may a continuous layer. An artisan can readily determine what falls within the scope of this limitation.

Also, the specification provides clear support that aids understanding. Page 3, lines 26- page 4, line 5, for example, describes formation of a sufficiently thin layer to form a discontinuous film. Page 5, lines 11-14, describes, among other things, formation of metal structures with ~10 nm characteristic lateral dimensions. Though unnecessary to understand

the claim language, these examples in the specification provide further support for the claim limitation.

Claims 7 and 18 stand rejected under 35 U.S.C. §112 as being indefinite for the use of improper Markush language. The proposed amendment has been made to address the rejection. It is believed that the claims would have been understood in their originally written form, but Applicants agree that the amended language places the claims in a better form. The scope of the claims remains the same.

Claims 1-8, 10 and 11 stand rejected under §103 as being obvious in view of Peng et al. et al. (U.S. Patent No. 5,895,223) in view of Przybysz (U.S. Patent No. 4,353,779). The rejection is respectfully traversed because neither Peng et al. nor Przybysz, alone or in combination, disclose or suggest at least the step of producing porous Group III-V material by etching a Group III-V surface having a thin discontinuous metal layer in a HF and oxidant solution. Applicants request reconsideration and withdrawal of the rejection.

Applicants note a fundamental flaw in the rejections is the failure of the Examiner to recognize the lack of <u>any</u> disclosure in the applicable references of the formation of porous Group III-V material. All of the cited references are merely directed to material removal processes, and not to the formation of porous Group III-V material. Applicant submits that the Examiner either misunderstands the references or fails to appreciate the difference between material removal processes and the formation of porous Group III-V material. Further, the Examiner has only cited references disclosing metal contacts and structures that do not contribute to any etching process. The Examiner has

failed to make a prima facie case of obviousness because there is not even a single applied reference that is directed to the formation of porous Group III-V material. None of the references applied produce porous material, each instead performs an etch to pattern a semiconductor quality Group III-V layer without altering the nature of the layer. The structures may have metal contacts and other common device features, but none of the material etching processes of the references are assisted by nanometer sized metal nanoparticles.

There are also additional defects in the rejection. The Office Action concludes that Przybysz suggests a modification of Peng et al. to use the etching solution of Przybysz on a nitride chip with partially metal-coated electrode as part of a porous Group III-V formation process. No such suggestion is provided by the teachings of Przybysz. The overall approaches of both Peng et al. and Przybysz are distinct from what is presently claimed, mainly the formation of porous Group III-V, and fail to support the position taken by the Examiner in the Office Action.

Peng et al. is directed to a wet-etching technique for etching nitride in which the rate of etching, the roughness of the etching surface, and the uniformity of the etching depth is controlled (col. 2, lns. 12-15). Accordingly, the reference discloses the steps of coating an electrode on the nitride chip, dipping the chip in electrolysis liquid, irradiating the nitride chip, and connecting the electrode to a second electrode (Claim 1). Although Peng et al. uses a metal electrode layer of Pt, the Examiner incorrectly points to the layer as corresponding to the claimed step of depositing a thin discontinuous layer of metal on a

Group III-V material surface. Peng et al. merely teaches partially coating a limited area on the chip, not a discontinuous layer. Further, Peng et al. does not disclose nor want a discontinuous layer over the whole chip in order to practice the particular etching method taught in the reference. Further still, the electrode is a continuous metal structure, not nanometer sized particles that contribute to the etching process. The metal layer of Peng et al. does not contribute to the etching process, and further, does not form porous Group III-V. In other words, Peng et al. does not teach at least the feature of forming porous Group III-V by etching a Group III-V surface having a discontinuous layer of metal in a HF and oxidant solution.

Przybysz is directed to wet chemical etching of Group III-V in the production of vias or recesses, such as in an integrated circuit. The primary stated goal of Przybysz is to provide an etching solution that is effective for producing predetermined and patterned vias in Group III-V without evolving a gaseous product (col. 1, line 66- col. 2, line 7). This is a device patterning technique, and has nothing to do whatsoever with forming porous Group III-V material. The Office Action states that one skilled in the art would have found it obvious to modify Peng et al. with the etching solution of Przybysz as part of a porous Group III-V formation process. The Office Action further states the motivation for the modification is that "the amount of F-ion [is] effective to allow sharp uniform etching without precipitation or gaseous evolution at the etching site and the etching solution acts as a particularly effective solvent solution for GaAs/Group III-V material". However, nothing in

this reference suggests the use of wet chemical etching in the formation of porous Group III-V material.

Claim 23 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Peng et al. et al. in view of Yoshikawa (U.S. Patent No. 5,990,605) and further in view of Przybysz. Applicants respectfully traverse and request reconsideration and withdrawal of the rejection for at least the reasons as stated above, and for at least the additional reason that Yoshikawa does not appear to remedy the deficiencies of Peng et al. and Przybysz.

The Examiner points to the electrode layer in Yoshikawa as corresponding to the claimed step of depositing metal on a Group III-V material surface in a thickness sufficient to prevent nucleation that forms nanometer sized metal particles and small enough to prevent formation of a continuous metal layer. This is incorrect. Yoshikawa has a standard thin metal contact. The metal contact of Yoshikawa plays no role whatsoever in the formation of the porous silicon in Yoshikawa. In fact, Yoshikawa forms the metal layer after porous semiconductor is formed. Therefore, Yoshikawa provides no suggestion to use a discontinuous metal layer in the formation of porous silicon or porous Group III-V.

As stated in column 1, lines 19-21, the thin metal electrode 15 is formed after the formation of the porous semiconductor layer 13. It is stated that the electron emission device "comprises a semiconductor layer 13 and a thin film metal electrode 15 which are formed, in turn, on a silicon layer 12". This is also emphasized in column 4, lines 58-62 where it is stated once again that the thin metal electrode is layered on the already formed porous silicon semiconductor layer 13. In Yoshikawa, therefore, the thin metal electrode is

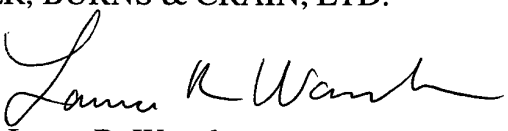
not at all part of the porous silicon formation process. Yoshikawa, therefore, includes no suggestion whatsoever of using a discontinuous metal layer for the formation of porous silicon or porous Group III-V, as required in independent claims 1, 12 and 23 in varying scope.

Applicants believe the above to be a complete and sufficient response. Applicants maintain the separate patentability of dependent claims but deem further response unnecessary in view of the above-identified deficiencies in the rejections.

For the foregoing reasons, applicants believe that this case is in condition for allowance, which is respectfully requested. The Examiner should call applicants' attorney if an interview would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

Laura R. Wanek
Registration No. 53,737

300 South Wacker Drive - Suite 2500
Chicago, Illinois 60606-6501
Telephone: (312) 360-0080
Facsimile: (312) 360-9315
Customer Number 24978
K:\1201\65872\Amendment A.doc